REMARKS

In the Official Action mailed 05 July 2007 and made final, the Examiner has rejected claims 1-33 under 35 U.S.C. §103(a) as being unpatentable over Bartkowiak *et al.* (US 5,771,362) in view of Wang *et al.* (US 7,028,134). Applicant responded on 5 October 2007, and requested reconsideration.

In the Advisory Action mailed 22 October 2007, the Examiner disagreed with the arguments presented, and further indicated for the first time, that "the passage in Bartkowiak et al. (US 5,771,362) at col. 5, lines 17-20 in the context of col. 5 lines 11-13, discusses the pipelining of function units for which control signals have been asserted, implying that the control of such units occurs in a parallel fashion."

Applicant again requests reconsideration, repeating the arguments presented on 5 October, and addressing the new comments presented in the Advisory Action.

Comments on Advisory Action

The passage referenced by the Examiner in the Advisory Action reads as follows:

> Preferably, each functional unit is configured to compute a result in a single clock cycle. However, other embodiments of DSP **10** are contemplated in which the functional units may be pipelined such that multiple clock cycles elapse during the performance of a particular instruction operation.

The cited passage does not relate to distribution of control words in parallel to routing units as suggested by the Examiner. The pipelining of functional units is well known technology that relies on instructions that are passed down the pipeline with the data, in series.

Furthermore, the comment by the Examiner that this passage implies "... that the control of such units [pipelined functional units] occurs in a parallel fashion," demonstrates that the Examiner may have been mistaken about the claim limitation at issue. In particular, the claim limitation at issue is the distribution of control words to routing units - not parallel control of functional units as the comment by the Examiner asserts.

Therefore, Applicant submits that the application should be allowed for the reasons stated below (previously submitted in response to the final office action).

Response to Official Action

Applicant submits that the *prima facie* case of unpatentability is based on a mistaken interpretation of the prior art, and requests reconsideration on that basis.

Claim 1 is reproduced here for reference and as representative of the other claims, with the limitation at issue underlined.

> 1. A data processing system, comprising:
>
> a plurality of functional units having respective inputs and outputs, and adapted to perform respective tasks using input data at the respective inputs and to supply output data at the respective outputs, within a cycle;
>
> a plurality of routing units, responsive to respective routing control signals, by which data is steered among inputs and outputs of the plurality of functional units, routing units in the plurality of routing units being coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets is different than another of said respective subsets; and
>
> control word distribution circuitry which supplies the routing control signals in parallel to the plurality of routing units to establish a route for a cycle, where the route includes applying data output in the cycle by a first functional unit in the plurality of functional units as input in the cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the cycle as input in the cycle to a third functional unit in the cycle.

In the response filed 9 April 2007, Applicant pointed out that neither reference shows the underlined "control word distribution circuitry" limitation. In the Office Action, the Examiner states that "the Bartkowiak *et al*. reference was cited for its teachings of such limitations" (Page 3).

Next, the Examiner states, with respect to the "control word distribution circuitry" limitation, that "in addition to the cited passages, Fig. 1 shows, or at least suggests, the routing of control signals #26A and #26B in parallel." (Page 3).

As a basis for this request for reconsideration, Applicant points out that the reference numbers 26A and 26B refer to data buses. See, column 4, lines 53-58 of Bartkowiak *et al.* The control words in the claims in the present application cannot be read on the data on the data buses 26A and 26B. The control signals for the interconnect in Bartkowiak *et al.* are supplied in series on interconnect control bus 30 from an instruction sequencer 16.

The "cited passages" referred to by the Examiner are found on page 6 of the Office Action, and include a single passage at column 2, lines 15-32. This cited passage is characterized in the Office Action as "discussing a dynamically configurable interconnect, in which an instruction filed specifies the interconnect configuration." (Page 6). However, this passage discusses a dynamically configurable interconnect only. It does not describe any structure corresponding to the claimed control word distribution circuitry. In fact, and unlike the claims, Bartkowiak *et al.* describes a system that supplies the control words for the dynamically configurable interconnect in series. Column 4, lines 23-39, reproduced here, of Bartkowiak *et al.* describe the bus interconnect 28 and the interconnect control bus 30, and their operation in series in response to an instruction sequencer:

> Bus interconnect **28** receives control signals upon an interconnect control bus **30** from instruction sequencer **16**. Instruction sequencer **16** asserts a particular control signal to cause transfer of data between a particular source and a particular destination. Deasserting the particular control signal inhibits transfer of data between the particular source and the particular destination. While the particular control signal is deasserted, a second control signal may be asserted to cause transfer of data from another source to the particular destination. The control signals upon interconnect control bus **30** are generated in response to a field of the instructions being executed by instruction sequencer **16**. The field specifies the control signals either in encoded or decoded format. Advantageously, bus interconnect **28** may be specified by the instructions being executed to be an optimal interconnection of the functional units of DSP **10** for the particular algorithm being performed.

Bartkowiak *et al*. therefore teaches supplying control words for the dynamically configurable bus interconnect 28 in series. It does not "show" and does not "suggest" supplying control words in parallel, as required by all the claims herein. Applicant requests reconsideration, because the Examiner is mistaken on this key point in the *prima facie* case.

Without reliance on this mistaken assertion, the Examiner's position that the claimed invention would have been obvious to a person of skill in the art is incomplete.

Bartkowiak *et al*. teaches a system that runs according to the classical sequential instruction processing approach, with a single dynamic interconnect that receives a control signal that is derived from each instruction to be processed in series. It cannot be expanded to suggest the present invention, in which there are a plurality of routing units operated in parallel, and receiving control words in parallel.

For the reasons set forth in the response filed on 9 April 2007, and for the reasons set forth above, Applicant submits that the rejection should be withdrawn.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (UNMI 1000-1).

Respectfully submitted,

Dated: 30 October 2007

/Mark A. Haynes/

Mark A. Haynes, Reg. No. 30,846

HAYNES BEFFEL & WOLFELD LLP
P.O. Box 366
Half Moon Bay, CA 94019
(650) 712-0340 phone
(650) 712-0263 fax